

CLAIMS

What is claimed is:

1. A method for self-routing a plurality of packets through a $2^n \times 2^n$ switch, the
5 switch having 2^n external output ports labeled with 2^n distinct binary output addresses in
the form of $b_1b_2\dots b_n$, and composed of a plurality of switching cells interconnected into a
k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \dots, \gamma(k)$
where γ is a mapping from the set $\{1, 2, \dots, k\}$ to the set $\{1, 2, \dots, n\}$, each of the packets
destined for a rectangular set of output addresses represented by a quaternary sequence $Q_1,$
10 Q_2, \dots, Q_n , where each Q_j is a quaternary symbol in any of the three values: ‘0-bound’,
‘1-bound’, and ‘bic平’, wherein each of the switching cells is a sorting cell associated with
the partial order “‘0-bound’ \prec ‘bic平’ \prec ‘1-bound’”, the method comprising
generating the routing tag $Q_{\gamma(1)}Q_{\gamma(2)}\dots Q_{\gamma(k)}$ for each of the packets with
reference to the guide and the destination output addresses of the packet, and
15 routing each of the packets through the network by using $Q_{\gamma(j)}$ in the routing
tag of the packet in the j-th stage cell, $1 \leq j \leq k$, to select an output or both outputs from the
j-th stage cell to emit the packet.

2. A $2^n \times 2^n$ self-routing switch comprising

an array of 2^n external input ports and an array of 2^n external output ports

with 2^n distinct binary output addresses in the form of $b_1b_2\dots b_n$ for routing a packet, the

packet being either a real data packet destined for a rectangular set of output addresses

5 represented by a quaternary sequence Q_1, Q_2, \dots, Q_n , where each Q_j is a quaternary symbol

having one of the values of ‘0-bound’, ‘1-bound’ or ‘bicast’, or being an idle packet having

no pre-determined destination output address,

a switch fabric having a plurality of switching cells interconnected into a

k-stage bit-permuting network which is characterized by the guide $\gamma(1), \gamma(2), \dots, \gamma(k)$,

10 where γ is a mapping from the set $\{1, 2, \dots, k\}$ to the set $\{1, 2, \dots, n\}$,

a tag generator circuit, coupled to the external input ports, for generating a

routing tag $1d_{\gamma(1)}d_{\gamma(2)}\dots d_{\gamma(k)}$ for the packet with reference to the guide of the bit-permuting

network and the destination address of the packet, and

a routing control circuit, coupled to the switching cells, for routing the

15 packet through the switch by using $1d_{\gamma(j)}$ in the routing tag in the j -th stage cell, $1 \leq j \leq k$, to

select an output from the j -th stage cell to emit the packet.